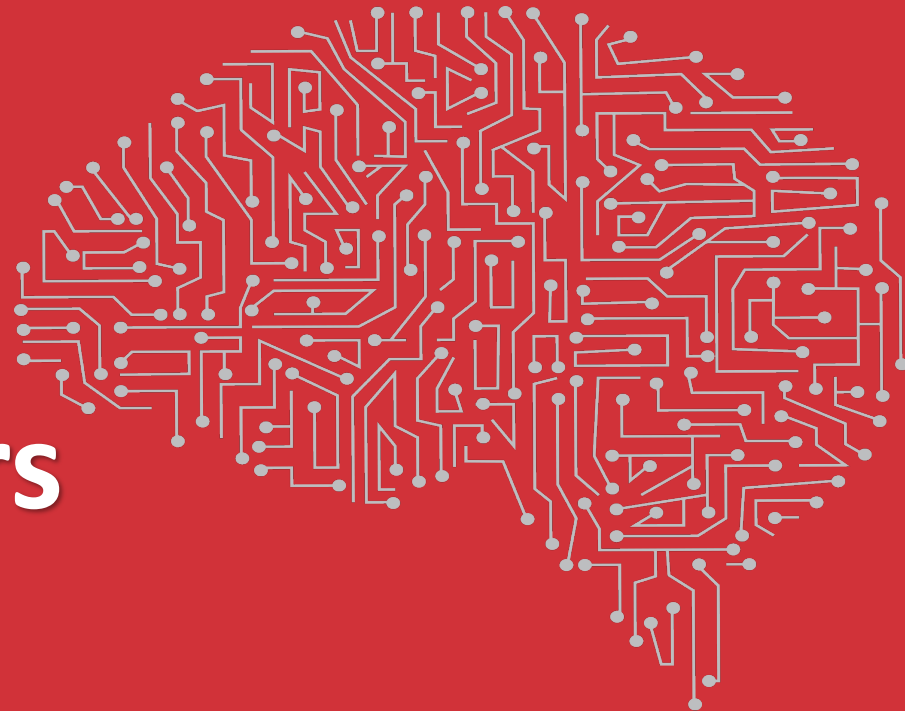


Grilování s M Comupters (2023)



4th Gen Intel® Xeon® Scalable Processors (Sapphire Rapids)

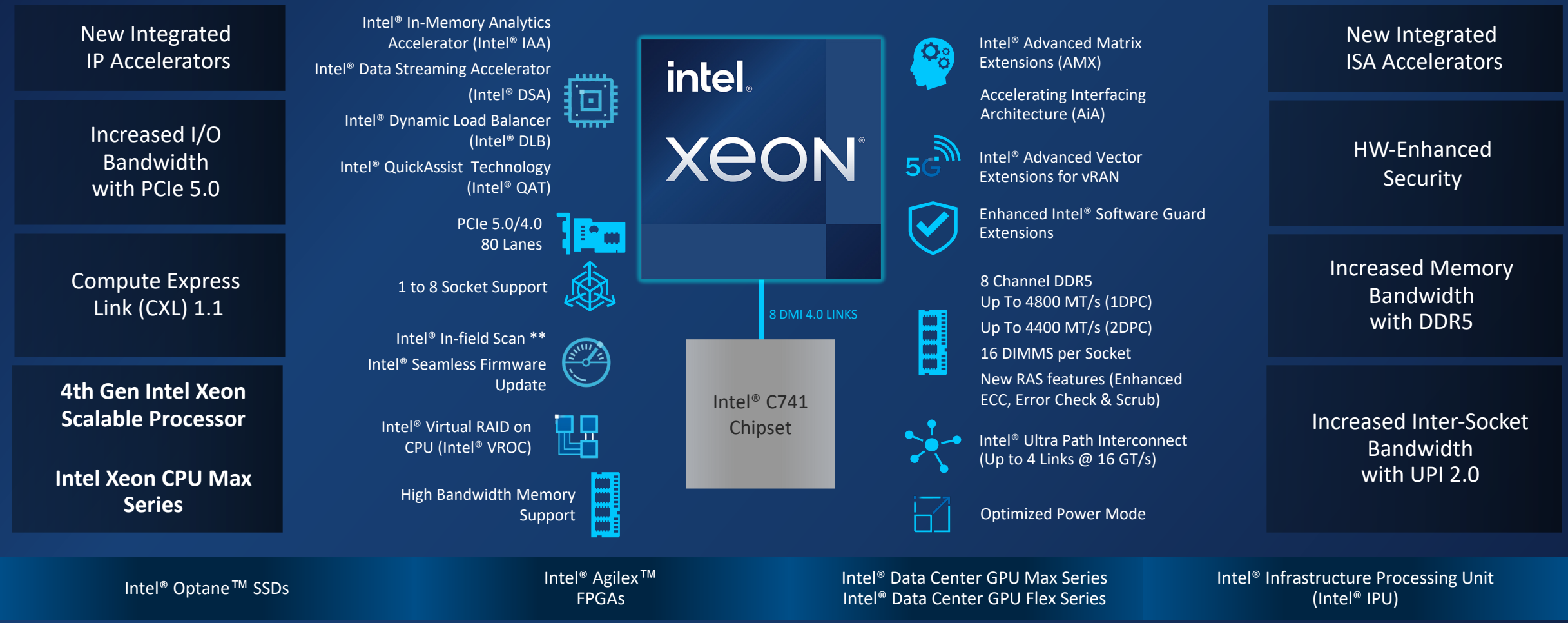
Intel® Xeon® MAX



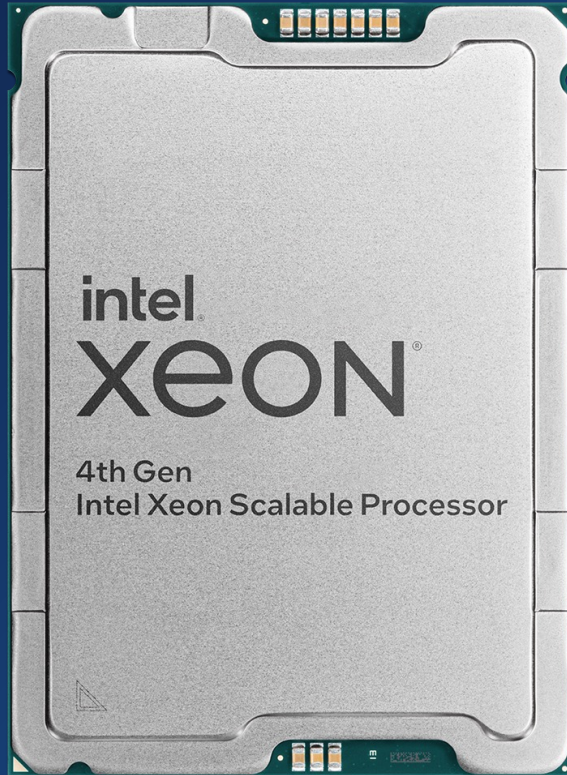
INTRODUCING

Intel's Most Feature Rich Server Platform

4th Gen Intel® Xeon® Scalable Processors and Intel® Xeon® CPU Max Series Processors



4th Gen Intel® Xeon® Scalable Processors



1 to 8 socket scalability

Up to 60 cores
per processor

Most built-in accelerators of any CPU

Increased memory bandwidth with DDR5

Increased I/O bandwidth with PCIe 5
80 lanes

Increased inter-socket bandwidth with UPI 2.0

Compute Express Link (CXL) 1.1

Hardware enhanced security

2S PERFORMANCE GENERAL PURPOSE

SKU Number	Cores	Base (GHz)	All Core Turbo (GHz)	Max Turbo (GHz)	Cache (MB)	TDP (Watts)	Maximum Scalability	DDR5 Memory Speed	UPI Links Enabled	Default DSA Devices	Default QAT Devices	Default DLB Devices	Default IAA Devices	Intel SGX Enclave Capacity (Per Processor)	Recommended Customer Pricing (RCP) in \$ US Dollars	Intel® On Demand Capable	Die Chop
8480+	56	2	3	3.8	105	350	2S	4800	4	1	1	1	1	512GB	\$10,710	✓	XCC
8470	52	2	3	3.8	105	350	2S	4800	4	1	0	0	0	512GB	\$9,359	✓	XCC
8468	48	2.1	3.1	3.8	105	350	2S	4800	4	1	0	0	0	512GB	\$7,214	✓	XCC
8460Y+	40	2	2.8	3.7	105	300	2S	4800	4	1	1	1	1	128GB	\$5,558	✓	XCC
8462Y+	32	2.8	3.6	4.1	60	300	2S	4800	3	1	1	1	1	128GB	\$5,945	✓	XCC
6448Y	32	2.1	3	4.1	60	225	2S	4800	3	1	0	0	0	128GB	\$3,583	✓	MCC
6442Y	24	2.6	3.3	4	60	225	2S	4800	3	1	0	0	0	128GB	\$2,878	✓	MCC
6444Y	16	3.6	4	4.1	45	270	2S	4800	3	1	0	0	0	128GB	\$3,622	✓	MCC
6426Y	16	2.5	3.3	4.1	37.5	185	2S	4800	3	1	0	0	0	128GB	\$1,517	✓	MCC
6434	8	3.7	4.1	4.1	22.5	195	2S	4800	3	1	0	0	0	128GB	\$2,607	✓	MCC
5415+	8	2.9	3.6	4.1	22.5	150	2S	4400	3	1	1	1	1	128GB	\$1,066	✓	MCC

2S MAINLINE GENERAL PURPOSE

8452Y	36	2	2.8	3.2	67.5	300	2S	4800	4	1	0	0	0	128GB	\$3,995	✓	XCC
6438Y+	32	2	2.8	4	60	205	2S	4800	3	1	1	1	1	128GB	\$3,141	✓	MCC
6430	32	2.1	2.6	3.4	60	270	2S	4400	3	1	0	0	0	128GB	\$2,128	✓	XCC
5420+	28	2	2.7	4.1	52.5	205	2S	4400	3	1	1	1	1	128GB	\$1,848	✓	MCC
5418Y	24	2	2.8	3.8	45	185	2S	4400	3	1	0	0	0	128GB	\$1,483	✓	MCC
4416+	20	2	2.9	3.9	37.5	165	2S	4000	2	1	1	1	1	64GB	\$1,176	✓	MCC
4410Y	12	2	2.8	3.9	30	150	2S	4000	2	1	0	0	0	64GB	\$563	✓	MCC

LIQUID COOLED GENERAL PURPOSE (-Q)

8470Q	52	2.1	3.2	3.8	105	350	2S	4800	4	1	0	0	0	512GB	\$9,410	✓	XCC
6458Q	32	3.1	4	4	60	350	2S	4800	3	1	0	0	0	128GB	\$6,416	✓	MCC

SINGLE SOCKET GENERAL PURPOSE (-U)

6414U	32	2	2.6	3.4	60	250	1S	4800	0	1	0	0	0	512GB	\$2,296	✓	XCC
5412U	24	2.1	2.9	3.9	45	185	1S	4400	0	1	0	0	0	128GB	\$1,113	✓	MCC
3408U	8	1.8	1.9	1.9	22.5	125	1S	4000	0	1	0	0	0	64GB	\$415		MCC

LONG-LIFE USE (IOT) GENERAL PURPOSE (-T)

4410T	10	2.7	3.4	4	26.25	150	2S	4000	2	1	0	0	0	64GB	\$624	✓	MCC
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Intel® Xeon® CPU Max Series / 4th Gen Intel® Xeon® Scalable Processors

[intel.com/xeon](https://www.intel.com/xeon)



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Max	=	9400 series	Gold	=	5000 series
Platinum	=	8000 series	Silver	=	4000 series
Gold	=	6000 series	Bronze	=	3000 series

Please visit "intel.com/xeon" or contact your Intel representative to obtain the latest product specifications. Intel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. All processors support Intel Virtualization Technology (Intel VT-x).

Y SKUs indicate support for Intel Speed Select Technology – Performance Profile 2.0 (Intel SST-PP).

+ General Purpose SKUs (Feature Plus) indicate products with 1 device per accelerator.

IMDB/ANALYTICS/VIRTUALIZATION OPTIMIZED (-H) – SOCKET SCALABLE

SKU Number	Cores	Base (GHz)	All Core Turbo (GHz)	Max Turbo (GHz)	Cache (MB)	TDP (Watts)	Maximum Scalability	DDR5 Memory Speed	UPI Links Enabled	Default DSA Devices	Default QAT Devices	Default DLB Devices	Default IAA Devices	Intel SGX Enclave Capacity (Per Processor)	Recommended Customer Pricing (RCP) in \$ US Dollars	Intel® On Demand Capable	Die Chop
8490H	60	1.9	2.9	3.5	112.5	350	8S	4800	4	4	4	4	4	512GB	\$17,000		XCC
8468H	48	2.1	3	3.8	105	330	8S	4800	4	4	4	4	4	512GB	\$13,923		XCC
8460H	40	2.2	3.1	3.8	105	330	8S	4800	4	4	0	0	4	512GB	\$10,710		XCC
8454H	32	2.1	2.7	3.4	82.5	270	8S	4800	4	4	4	4	4	512GB	\$6,540		XCC
8450H	28	2	2.6	3.5	75	250	8S	4800	4	4	0	0	4	512GB	\$4,708		XCC
8444H	16	2.9	3.2	4	45	270	8S	4800	4	4	0	0	4	512GB	\$4,234		XCC
6448H	32	2.4	3.2	4.1	60	250	4S	4800	3	1	2	2	1	512GB	\$3,658		MCC
6418H	24	2.1	2.9	4	60	185	4S	4800	3	1	0	0	1	512GB	\$2,065		MCC
6416H	18	2.2	2.9	4.2	45	165	4S	4800	3	1	0	0	1	512GB	\$1,444		MCC
6434H	8	3.7	4.1	4.1	22.5	195	4S	4800	3	1	0	0	1	512GB	\$3,070		MCC

5G / NETWORKING OPTIMIZED (-N)

8470N	52	1.7	2.7	3.6	97.5	300	2S	4800	4	4	4	4	0	128GB	\$9,520	✓	XCC
8471N	52	1.8	2.8	3.6	97.5	300	1S	4800	4	4	4	4	0	128GB	\$5,171	✓	XCC
6438N	32	2	2.7	3.6	60	205	2S	4800	3	1	2	2	0	128GB	\$3,351	✓	MCC
6428N	32	1.8	2.5	3.8	60	185	2S	4000	3	1	2	2	0	128GB	\$3,200	✓	MCC
6421N	32	1.8	2.6	3.6	60	185	1S	4400	3	1	2	2	0	128GB	\$2,368	✓	MCC
5418N	24	1.8	2.6	3.8	45	165	2S	4000	3	1	2	2	0	128GB	\$1,664	✓	MCC
5411N	24	1.9	2.8	3.9	45	165	1S	4400	3	1	2	2	0	128GB	\$1,232	✓	MCC

CLOUD OPTIMIZED IaaS (-P) / SaaS (-V) / Media (-M)

8468V	48	2.4	2.9	3.8	97.5	330	2S	4800	3	1	1	1	1	128GB	\$7,121	✓	XCC
8458P	44	2.7	3.2	3.8	82.5	350	2S	4800	3	1	1	1	1	512GB	\$6,759	✓	XCC
8461V	48	2.2	2.8	3.7	97.5	300	1S	4800	0	1	1	1	1	128GB	\$4,491	✓	XCC
6438M	32	2.2	2.8	3.9	60	205	2S	4800	3	1	0	0	1	128GB	\$3,273	✓	MCC

STORAGE & HYPERCONVERGED INFRASTRUCTURE (HCI) OPTIMIZED (-S)

6454S	32	2.2	2.8	3.4	60	270	2S	4800	4	4	4	4	0	128GB	\$3,157	✓	XCC
5416S	16	2	2.8	4	30	150	2S	4400	3	1	2	2	0	128GB	\$944	✓	MCC

HPC OPTIMIZED (Intel® Xeon® CPU Max Series)

9480	56	1.9	2.6	3.5	112.5	350	2S	4800	4	4	0	0	0	512GB	\$12,980		XCC
9470	52	2	2.7	3.5	105	350	2S	4800	4	4	0	0	0	512GB	\$11,590		XCC
9468	48	2.1	2.6	3.5	105	350	2S	4800	4	4	0	0	0	512GB	\$9,900		XCC
9460	40	2.2	2.7	3.5	97.5	350	2S	4800	3	4	0	0	0	128GB	\$8,750		XCC
9462	32	2.7	3.1	3.5	75	350	2S	4800	3	4	0	0	0	128GB	\$7,995		XCC

XCC = Extreme Core Count. MCC = Medium Core Count.

Unless noted, all 8400, 6400 and 5400 processors, include support for Intel Speed Select technology (Intel SST) featuring Intel SST Base Frequency (SST-BF), Intel SST Core Power (SST-CP) and Intel SST Turbo Frequency (SST-TF) capabilities.

Availability of accelerators varies depending on SKU. Visit the "Intel Product Specifications" page for additional product details. <https://ark.intel.com/content/www/us/en/ark.html>

Intel may make changes to specifications and product descriptions at any time, without notice.

Intel Optimized Tools for 4th Gen Intel® Xeon® Scalable Processors

Tools for developers to take advantage and enable onboard accelerators

Intel® oneAPI Math Kernel Library (oneMKL)
for HPC & technical compute

Intel® oneAPI Deep Neural Network Library
(oneDNN) for deep learning training +
inference

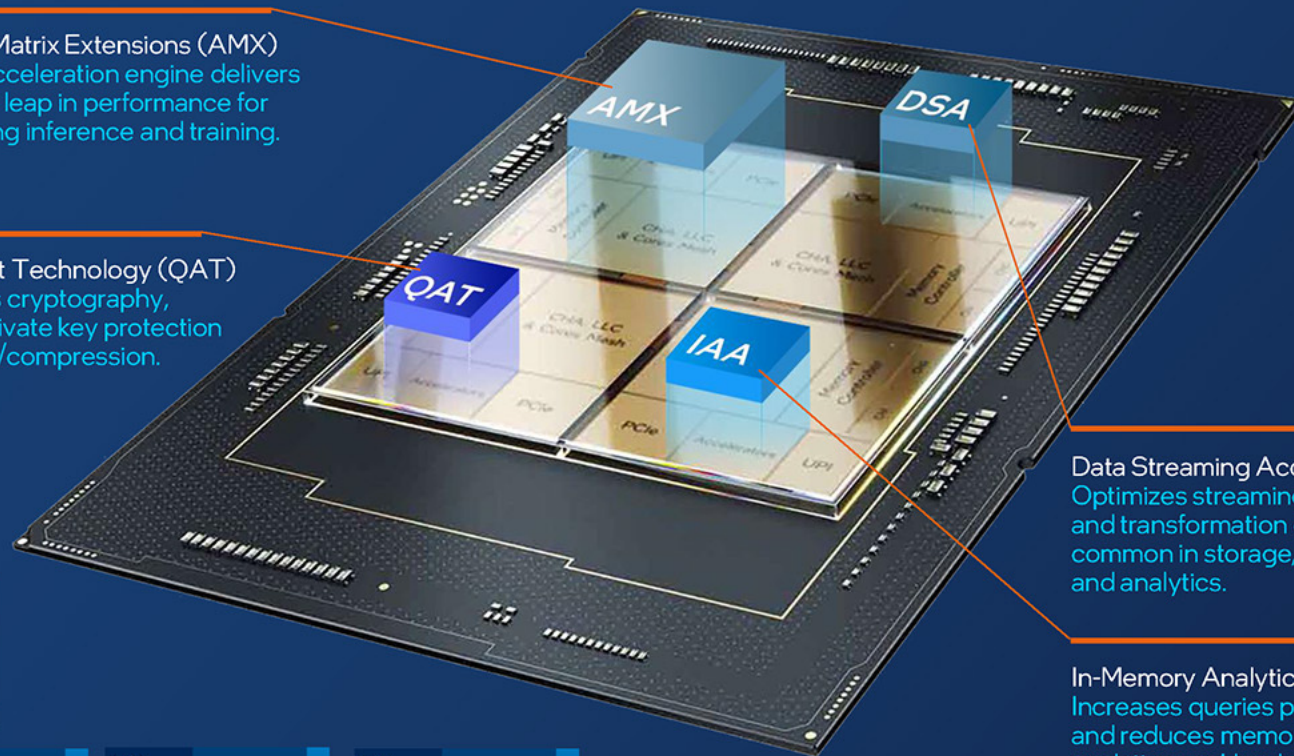
Intel® Query Processing Library (Intel® QPL)*
& Intel® Data Mover Library (Intel® DML)*
for query processing, compression &
data movement

Compilers, libraries & analysis tools
support instruction sets (such as AMX,
AVX2 & AVX512) to unleash performance
gains, including faster training & inference
for AI workloads

Intel® VTune™ Profiler helps locate the most
time-consuming parts of code and identify the
most significant issues affecting application
performance, including memory

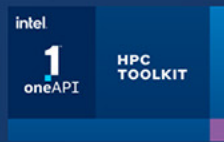
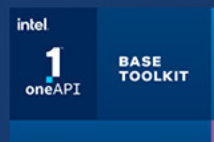
Advanced Matrix Extensions (AMX)
Built-in AI acceleration engine delivers
a significant leap in performance for
deep learning inference and training.

Quick Assist Technology (QAT)
Accelerates cryptography,
including private key protection
and data de/compression.



Data Streaming Accelerator (DSA)
Optimizes streaming data movement
and transformation operations
common in storage, networking,
and analytics.

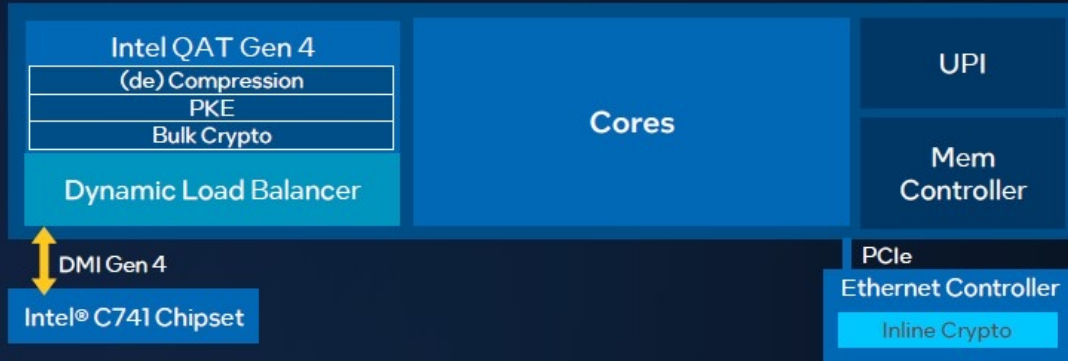
In-Memory Analytics Accelerator (IAA)
Increases queries per second
and reduces memory footprint for
analytics workloads



Intel® Accelerator Engines

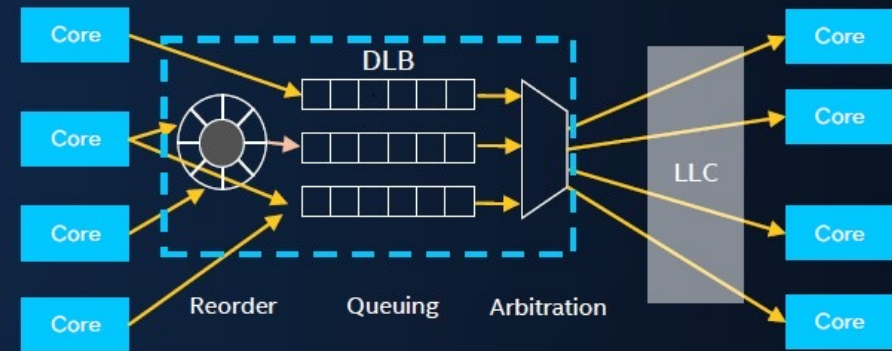
New Integrated IP

Intel® QuickAssist Technology (Intel® QAT)



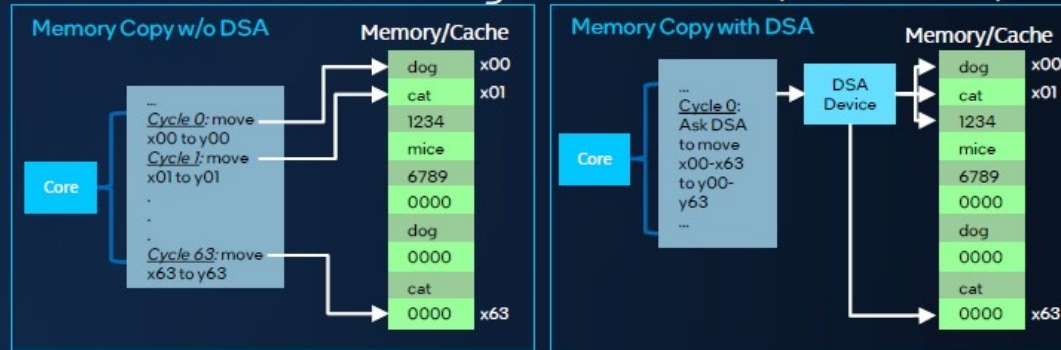
Customer Usages: Network Secure Gateway, CDN, Data Compression (L1/L9)

Intel® Dynamic Load Balancer (Intel® DLB)



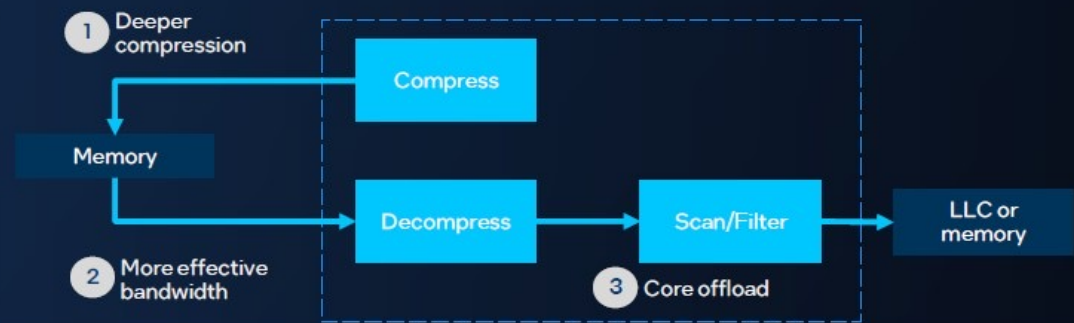
Customer Usages: Load Balancing, Queue Management, Packet Prioritization

Intel® Data Streaming Accelerator (Intel® DSA)



Customer Usages: High Perf Enterprise/Distributed Storage, Data Analytics

Intel® In-Memory Analytics Accelerator (Intel® IAA)



Customer Usages: In-Memory Databases, Big Data Analytics, Databases

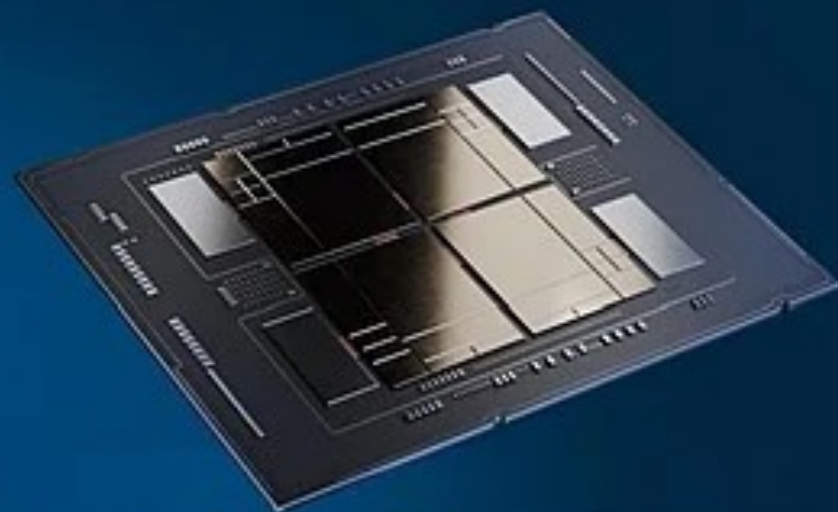
Intel Accelerator Engines by Processor Generation

Intel® Xeon® architecture has included purpose-built workload acceleration across Xeon generations

	Intel® Xeon® Scalable processors (Sky Lake)	2nd Gen Intel® Xeon® Scalable processors (Cascade Lake)	3rd Gen Intel® Xeon® Scalable processors (Ice Lake)	4th Gen Intel® Xeon® Scalable processors (Sapphire Rapids)
Intel® Advanced Vector Extensions 512 (Intel® AVX-512)	X	X	X	X
Intel® Crypto Acceleration			X	X
VNNI, BF16 (Intel® Deep Learning Boost)		X	X	X
Intel® Advanced Vector Extensions (Intel® AVX) for vRAN				X
Intel® Advanced Matrix Extensions (Intel® AMX)				X
Intel® Volume Management Device		X	X	X
Intel® Control-Flow Enforcement Technology (Intel® CET)				X
Intel® Software Guard Extensions (Intel® SGX)			X	X
Intel® Trust Domain Extensions (Intel® TDX)				Limited
Intel® Speed Select Technology (Intel® SST)		X	X	X
Intel® Data Direct I/O Technology (Intel® DDIO)	X	X	X	X
Intel® Dynamic Load Balancer (Intel® DLB)				X
Intel® QuickAssist Technology (Intel® QAT) (integrated)				X
Intel® Data Streaming Accelerator (Intel® DSA)				X
Intel® In-Memory Analytics Accelerator (Intel® IAA)				X



Only x86 CPU with High Bandwidth Memory



	64GB HBM2e	up to 112.5MB shared LLC	DDR5 8 channels per CPU @ 4800MT/s (SDPC) / 16 DIMMs per socket
~1TB/s memory BW			
>1GB/core HBM memory capacity			

* Relative performance ISO TDP and core count

Memory modes

HBM Only

Workloads < 64GB capacity

No code change
No DDR

System boots
and operates with
HBM only

HBM

HBM Flat Mode

Flat Mem Regions w/ HBM & DRAM
Workloads > 64GB capacity

Code change may be
needed to optimize perf

Provides flexibility for
applications that require
large memory capacity

HBM

DDR

HBM Caching Mode

DRAM backed cache
Improved performance for workloads > 64GB capacity

No code change
HBM Caches DDR

Blend of both prior modes. Whole
applications may fit in HBM cache
Blurs line between cache and memory

HBM

DDR

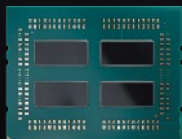
intel

Under Embargo until November 9, 2022, 6 am PT

AMD EPYC™ PROCESSOR JOURNEY

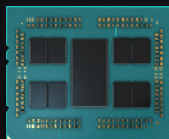
Four Generations of On-Time Execution

1st Gen EPYC™



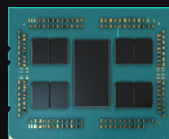
General Purpose
"Naples"

2nd Gen EPYC™

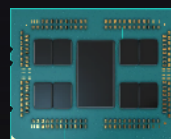


General Purpose
"Rome"

3rd Gen EPYC™

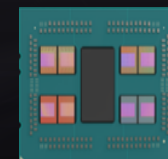


General Purpose
"Milan"

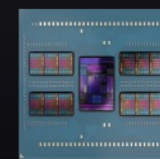


Technical
"Milan-X"

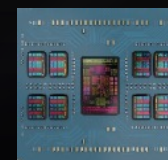
4th Gen EPYC™



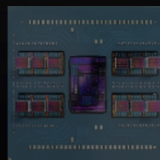
General Purpose
"Genoa"



Cloud Native
"Bergamo"



Technical
"Genoa-X"

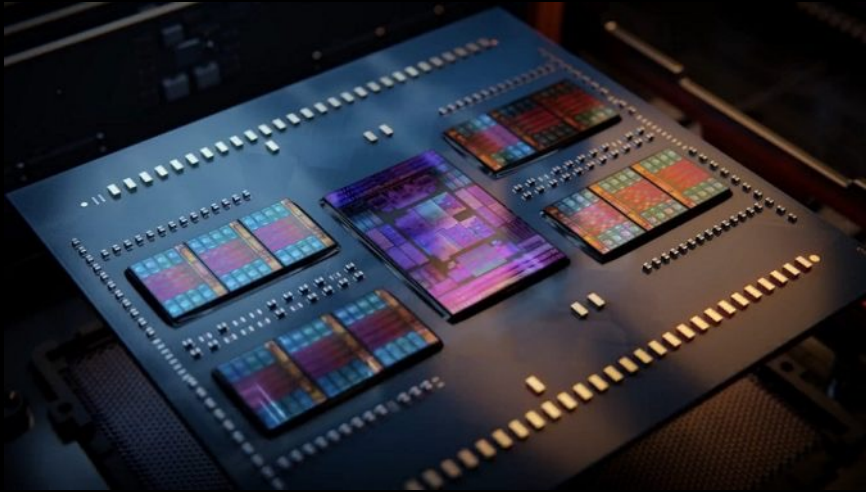


Telco/Edge
"Siena"

2017

2023

Introducing 4th Gen AMD EPYC™ Processors



AMD Epyc 9004
“GENOA”

“Zen 4” / “Genoa” SP5 SoC Architecture*

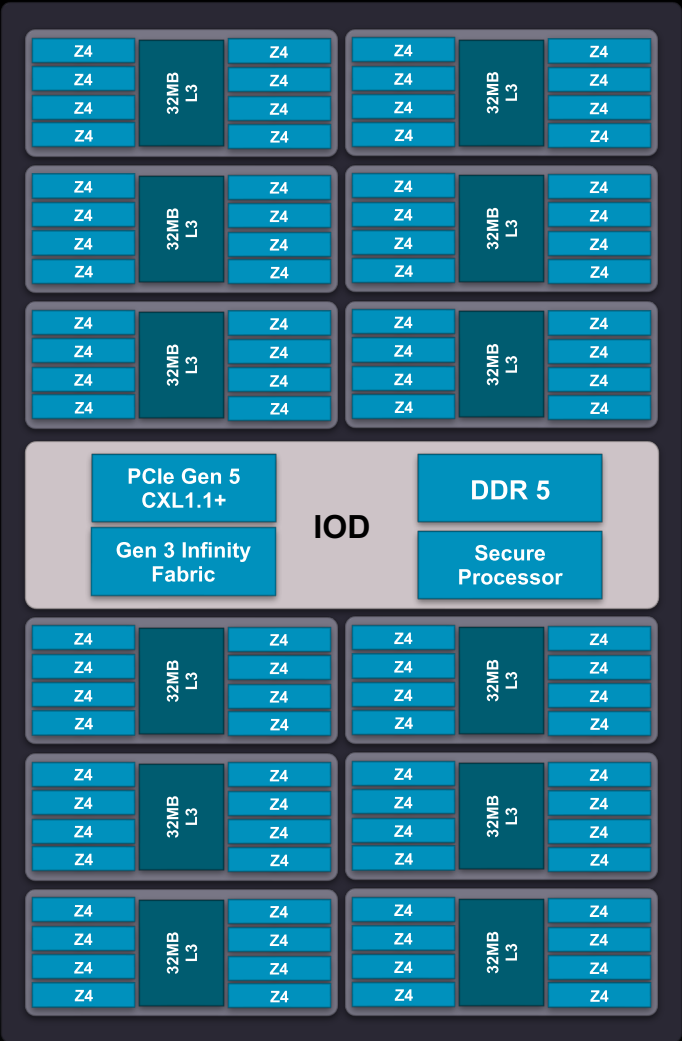


COMPUTE

- AMD “Zen 4” x86 cores (Up to 12 CCDs / 96 cores / 192 threads)
- 1MB L2/Core, up to 32MB L3/CCD
- ISA updates: BFLOAT16, VNNI, AVX-512 (256b data path)
- Memory addressability with 57b/52b Virtual/Physical Address
- Updated IOD and internal Gen3 Infinity Fabric architecture with up to 32Gbps transfer rate for die-to-die communication
- Target TDP range: ~200W to ~400W
- Updated RAS

MEMORY

- 12 channel DDR5 with ECC support up to 4800 MHz
- Option for 2, 4, 6, 8, 10, 12 channel memory interleaving
- RDIMM, 3DS RDIMM
- Up to 2 DIMMs/channel capacity of 6TB/socket (256GB 3DSDIMMs)



BLUE indicates significant update from “Zen 3” / “Milan”

I/O

- Up to 160 IO lanes (2P) of PCIe® Gen5, with speeds up to 32Gbps, bifurcations supported down to x1
- Up to 12 bonus PCIe Gen3 lanes in 2P config (8 lanes 1P)
- 32 IO lanes for SATA
- SDCI (Smart Data Cache Injection)
- 64 IO Lanes support CXL1.1+ Type 3 (Compute Express Link) with bifurcations supported down to x4 (4-ports)

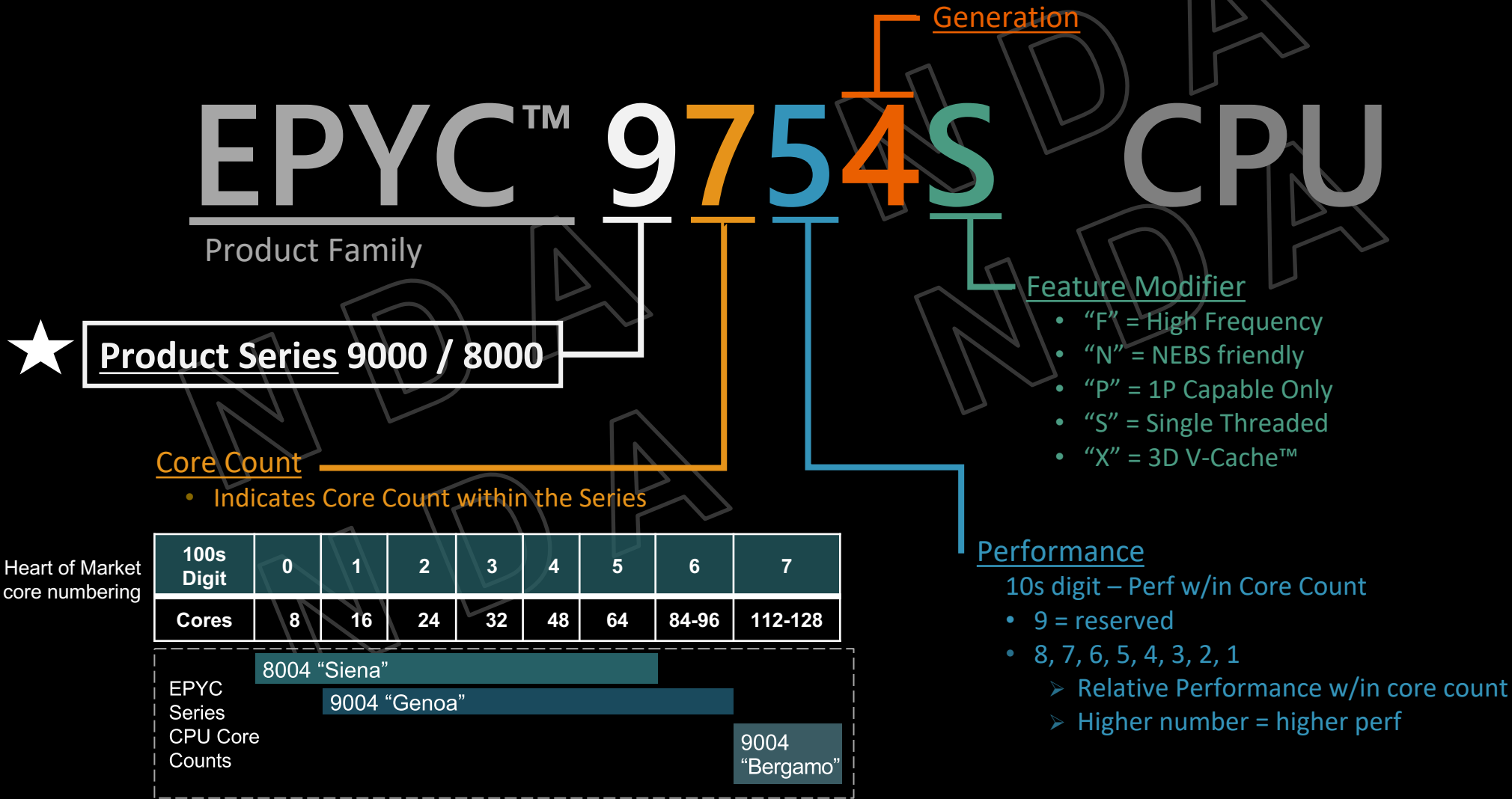
SP5 PLATFORM

- New socket, increased power delivery and VR
- Up to 4 links of Gen 3 Infinity Fabric™ with speeds of up to 32Gbps
- Flexible topology options
- Server Controller Hub (USB, UART, SPI, I2C, etc.)

SECURITY FEATURES

- Dedicated Security Subsystem with enhancements
- Hardware Root-of-Trust, Secure Boot
- SME (Secure Memory Encryption)
- SEV-ES (Secure Encrypted Virtualization & Register Encryption)
- SEV-SNP (Secure Nested Paging), AES-256-XTS with more encrypted VMs

AMD EPYC™ 9004 / 8004 Series - Processor Naming Convention



AMD EPYC™ 9004 CPUs

OPN Buckets

Cloud Native Optimized

9754
9754S
9734

AMD 3D V- Cache™

9684X
9384X
9184X

Perf / Core Optimized

9474F
9374F
9274F
9174F

Standard CPUs

9654
9634
9554
9534
9454
9354
9334
9254
9224
9124

1P Optimized

9654P
9554P
9454P
9354P

Core Count Grouped CPUs

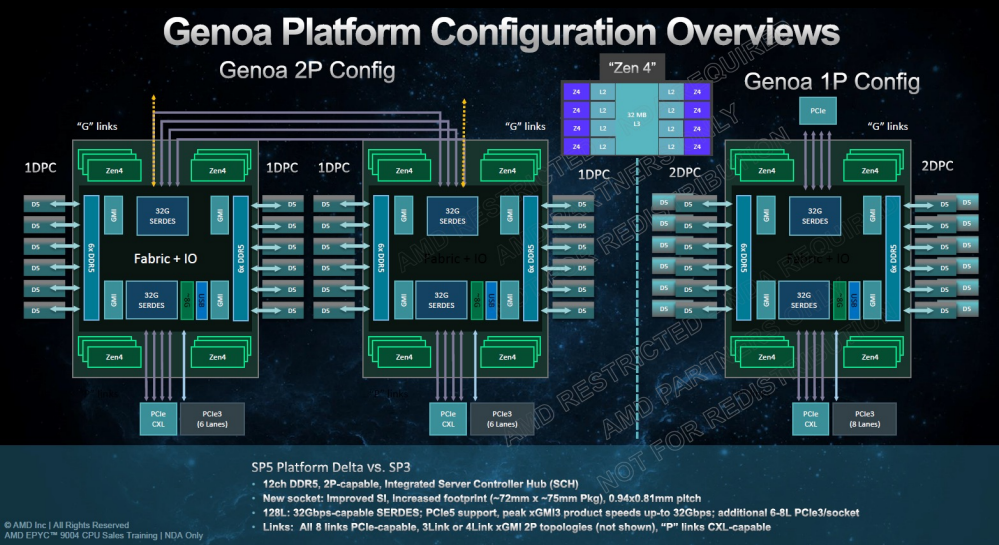
Standard CPUs

112C - 128C	9754
	9754S
	9734
84C - 96C	9684X
	9654
	9634
64C	9554
	9534
48C	9474F
	9454
32C	9384X
	9374F
	9354
	9334
24C	9274F
	9254
	9224
16C	9184X
	9174F
	9124

1P Optimized

9654P – 96c
9554P – 64c
9454P – 48c
9354P – 32c





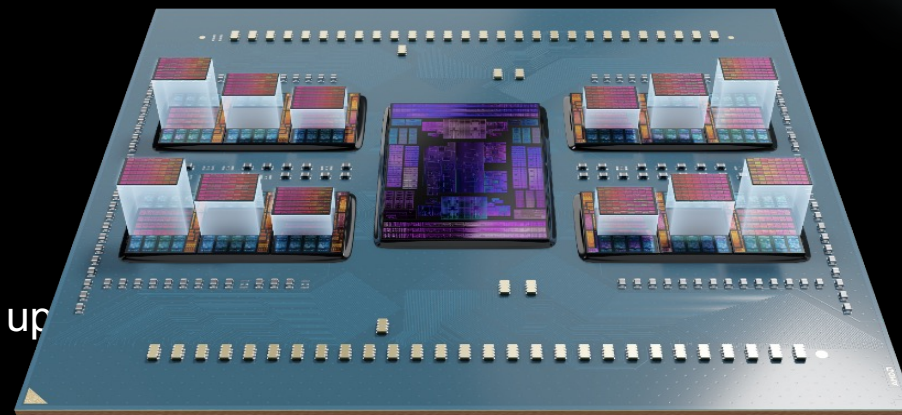
AMD Epyc 9004

“GENOA-X”

Designed for High Cache per Core
And Technical Compute Workloads

“GENOA-X” WITH AMD 3D V-CACHE™ TECHNOLOGY

- “Genoa-X” will be the 2nd Generation AMD CPU built with true 3D die stacking
 - Cu-Cu bond. No solder bumps.
 - Uses same CCD cores as non-stacked “Genoa” CPU
 - Socket, Infrastructure, BIOS and Software compatible with “Genoa”
 - Relieves memory bandwidth pressure and reduces latency
- AMD 3D V-Cache is designed for dramatic out-of-the-box performance up across a range of workloads including Commercial HPC apps
 - Electronic Design Automation
 - Computations Fluid Dynamics
 - Relational Databases
- “Genoa-X” is designed to expand workload coverage as ISVs optimize for large cache.



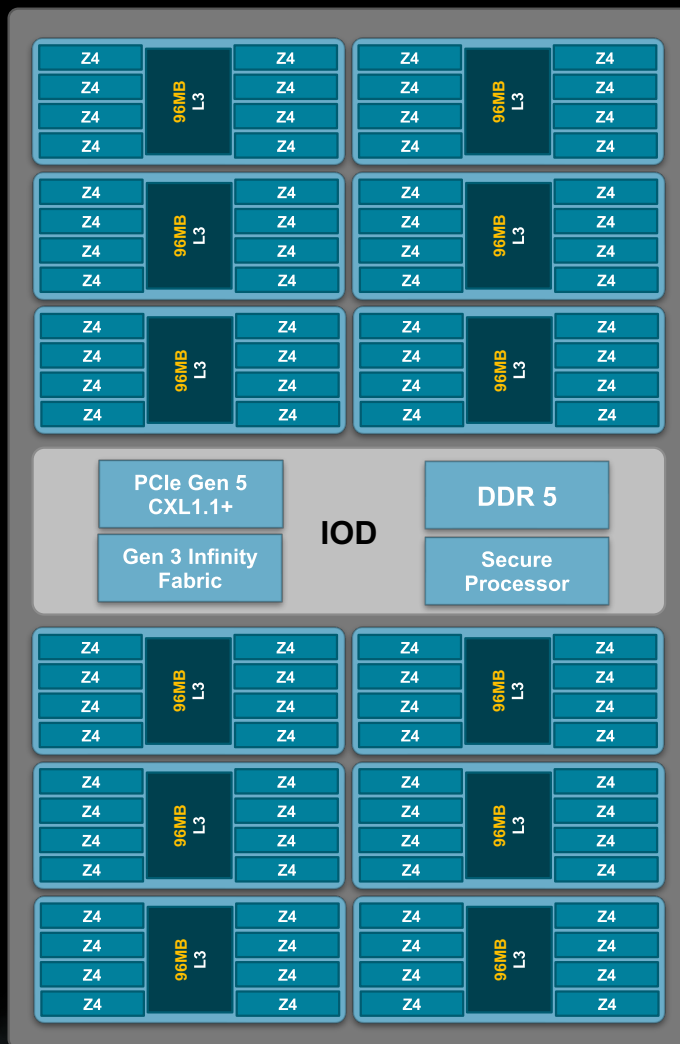
'GENOA-X' SP5 AT A GLANCE

COMPUTE

- AMD "Zen4" x86 cores (Up to 12 CCDs / 96 cores / 192 threads)
- 1MB L2/Core, **96MB L3/CCD / Total up to 1152MB L3**
- ISA updates: BFLOAT16, VNNI, AVX-512 (256b data path)
- Memory addressability with 57b/52b Virtual/Physical Address
- Updated IOD and internal AMD Gen3 Infinity Fabric™ architecture with increased die-to-die bandwidth
- Target TDP range: Up to 400W (cTDP)
- Updated RAS

MEMORY

- 12 channel DDR5 with ECC up to 4800 MHz
- Option for 2, 4, 6, 8, 10, 12 channel memory interleaving
- RDIMM, 3DS RDIMM
- Up to 2 DIMMs/channel capacity of 6TB/socket (256GB 3DS RDIMMs)



BLUE indicates significant update from "Milan"
ORANGE indicates difference from "Genoa"

I/O

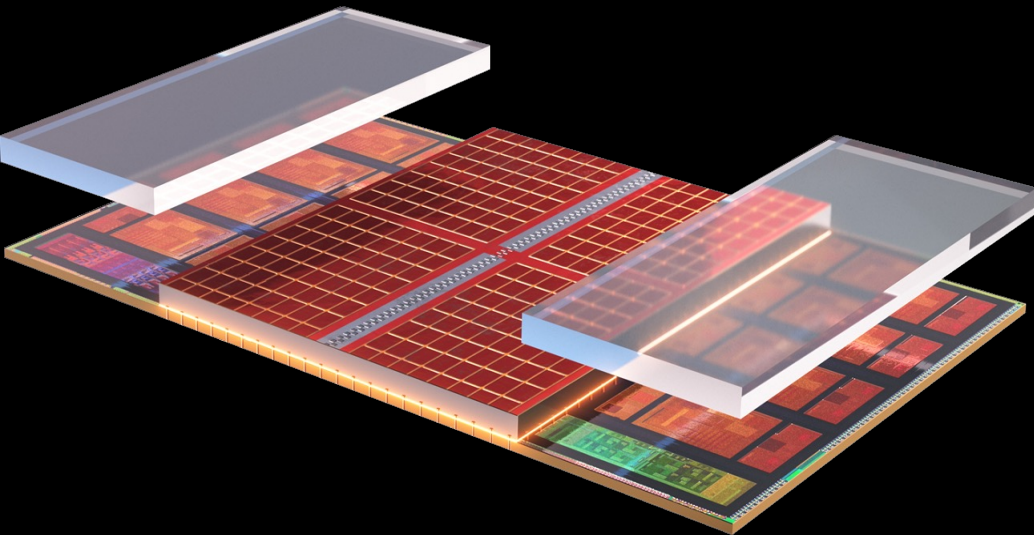
- Up to 160 IO lanes (2P) of PCIe® Gen5, with speeds up to 32Gbps, bifurcations supported down to x1
- Up to 12 bonus PCIe Gen3 lanes in 2P config (8 lanes—1P)
- Up to 32 IO lanes for SATA
- SDCI (Smart Data Cache Injection)
- 64 IO Lanes support CXL1.1+ with bifurcations supported down to x4

SP5 PLATFORM

- New socket, increased power delivery and VR
- Up to 4 links of Gen3 AMD Infinity Fabric™ with speeds of up to 32Gbps
- Flexible topology options
- Server Controller Hub (USB, UART, SPI, I2C, etc.)

SECURITY

- Dedicated Security Subsystem with enhancements
- Hardware Root-of-Trust



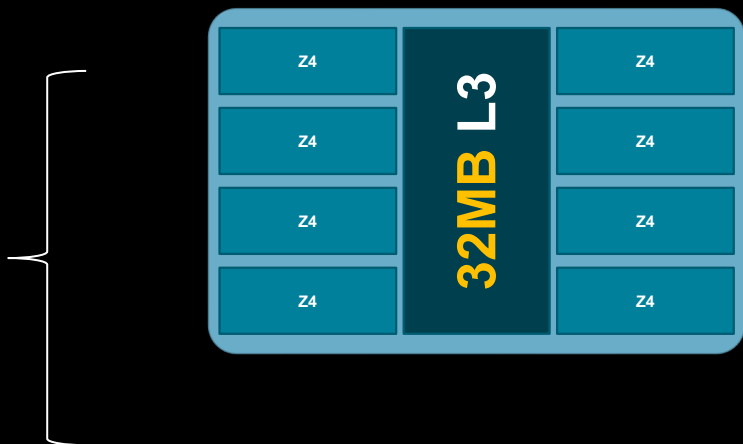
AMD Epyc 9004 – 97X4

“BERGAMO”

Optimized for Cloud Native Workloads

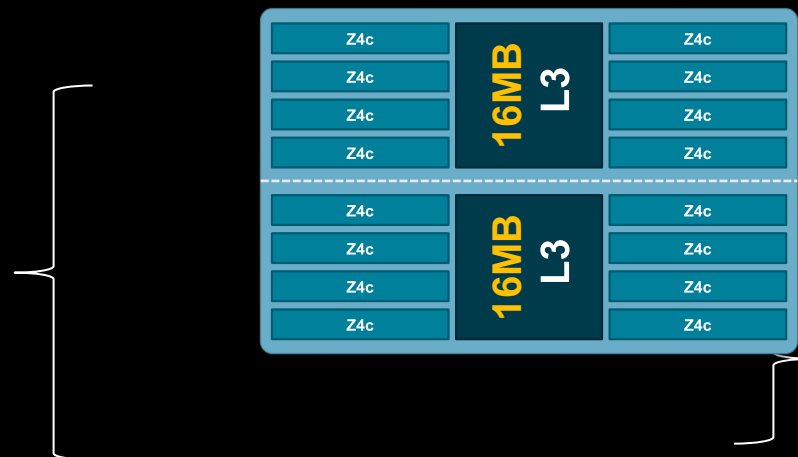
“Zen4c” Chiplets

“Zen4” Chiplet



- Optimized for perf/core
- 1MB L2 cache per core
- 32MB of shared L3 cache per CCD

“Zen4c” Chiplet



- Optimized for perf/watt
- 1MB L2 cache per core
- 16MB of shared L3 cache per CCX
- 32MB of shared L3 cache per CCD

Logically Similar (same ISA, L1 & L2 cache)
Implementation changes in “Zen4c” are transparent from SW perspective

4TH GEN EPYC WITH AMD BERGAMO

COMPUTE

- AMD “Zen4c” x86 cores (Up to 8 CCDs / Up to **128** cores / **256** threads)
 - 1MB L2/Core, **2x 16MB L3 CCX per CCD**
 - ISA updates: BFLOAT16, VNNI, AVX-512 (256b data path)
 - Memory addressability with 57b/52b VA/PA
-
- Updated IOD and internal AMD Gen3 Infinity Fabric™ architecture with increased die-to-die bandwidth
-
- TDP range: up to 400W (cTDP)
-
- Updated RAS

MEMORY

- 12 channel DDR5 with ECC up to 4800 MHz
 - Option for 2, 4, 6, 8, 10, 12 channel memory interleaving
-
- RDIMM, 3DS RDIMM
-
- Up to 2 DIMMs/channel capacity of 12TB per 2 socket system (based on 256GB 3DS DIMMs with 2 DIMMs per Channel support)



ORANGE indicates difference from “Zen4” and “Zen4c”

I/O

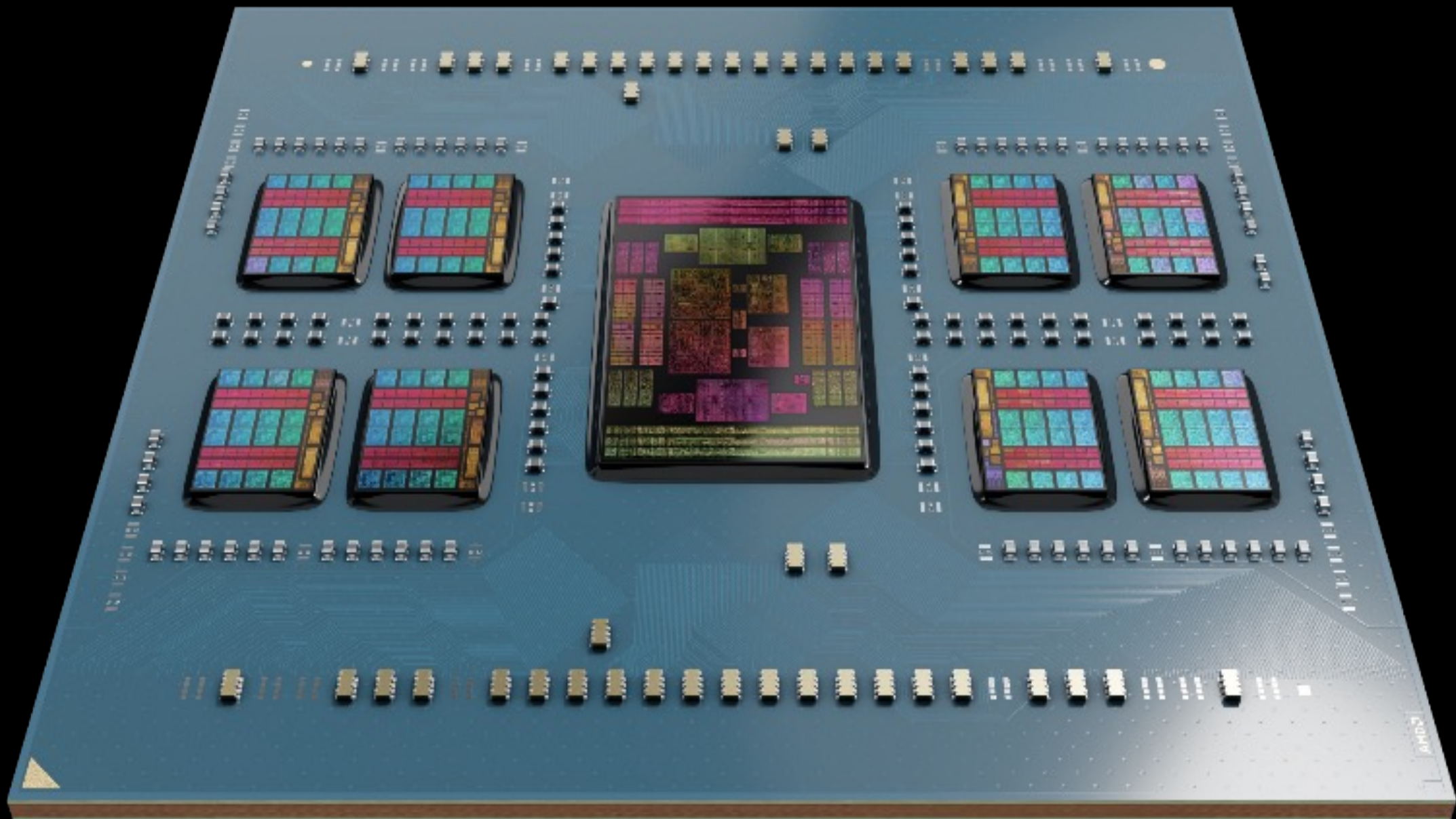
- Up to 160 IO lanes (2P) of PCIe® Gen5, with speeds up to 32Gbps, bifurcations supported down to x1
 - Up to 12 bonus PCIe Gen3 lanes in 2P config (8 lanes 1P)
 - 32 IO lanes for SATA
 - SDCI (Smart Data Cache Injection)
-
- 64 IO Lanes support CXL™1.1+ with bifurcations supported down to x4

SP5 PLATFORM

- New socket, increased power delivery and VR
 - Up to 4 links of Gen3 AMD Infinity Fabric™ with speeds of up to 32Gbps
 - Flexible topology options
-
- Server Controller Hub (USB, UART, SPI, I2C, etc.)

SECURITY FEATURES

- Dedicated Security Subsystem features with enhancements
- Hardware Root-of-Trust





JEDEC Industry Standard Specifications

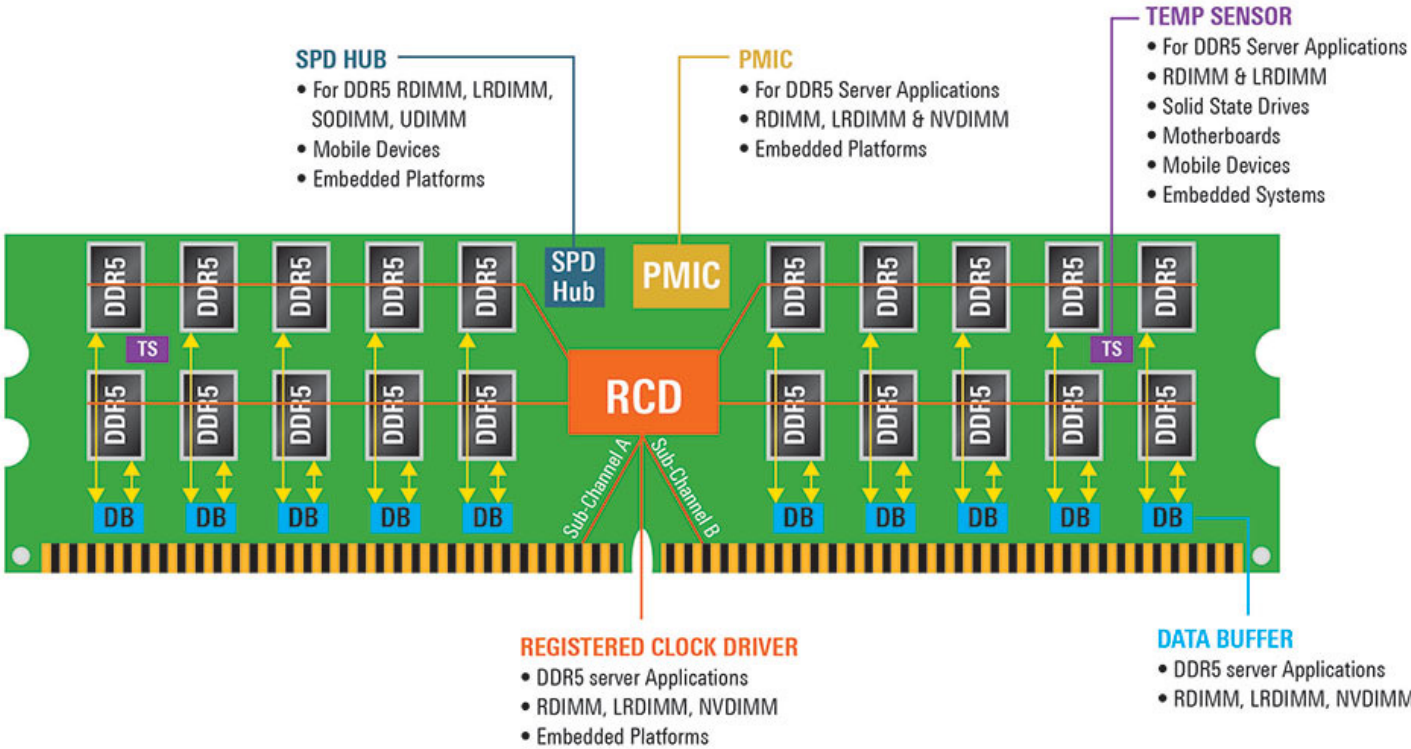
Description		DDR5
Data Rates (Speed in MT/s)		4000, 4400, 4800, 5200, 5600, 6000, 6400 MT/s
Monolithic DRAM Densities (Gbit)		8Gb, 16Gb, 24Gb, 32Gb, 48Gb, 64Gb
Package Type and Ballout (x4, x8 / x16)		BGA, 3DS TSV (78, 82 / 102)
Interface	Voltage (V _{DD} / V _{DDQ} / V _{PP})	1.1 / 1.1 / 1.8 V
	Internal V _{REF}	V _{REFDQ} , V _{REFCA} , V _{REFCS}
	Command/Address	POD (Pseudo Open Drain)
	Equalization	DFE (Dynamic Feedback Equalization)
	Burst Length	BL16 / BC8 / BL32 (optional)
Core Architecture	Number of Banks	<u>32 Banks (8 Bank Groups)</u> 8 BG x 4 banks (16-64Gb x4/x8) 8 BG x 2 banks (8Gb x4/x8) <u>16 Banks (4 Bank Groups)</u> 4 BG x 4 banks (16-64Gb x16) 4 BG x 2 banks (8Gb x16)
	Page Size (x4 / x8 / x16)	1KB / 1KB / 2KB
	Prefetch	16n
	DCA (Duty Cycle Adjustment)	DQS and DQ
	Internal DQS Delay Monitoring	DQS interval oscillator
	ODECC (On-die ECC)	128b+8b SEC error check and scrub
	CRC (Cyclic Redundancy Check)	Read/Write
	ODT (On-die Termination)	DQ, DQS, DM, CA bus
	MIR ("Mirror" pin)	Yes
	Bus Inversion	Command/address inversion (CAI)
	CA Training, CS Training	CA training, CS training
	Write Leveling Training Modes	Improved
	Read Training Patterns	Dedicated MRs for user-defined serial, clock, and <u>LFSR</u> - generated training patterns
	Mode registers	Up to 256 x 8 bits
	PRECHARGE Commands	All bank, per bank, and same bank
	REFRESH Commands	All bank and same bank
	Loopback Mode	Yes

PMIC

DDR5 modules feature Power Management Integrate Circuits (PMIC for short), which help regulate the power required by the various components of the memory module (DRAM, Register, SPD hub, etc). For server class modules the PMIC uses **12V**, and for PC class modules the PMIC uses **5V**. This makes for better power distribution than previous generations, improves signal integrity, and reduces noise.

SPD Hub

DDR5 utilizes a new device integrating the Serial Presence Detect (SPD) EEPROM with additional hub features, managing access to the external controller and decoupling the memory load on the internal bus from external



Key Features	Key Applications
<ul style="list-style-type: none"> • PCIe® 5.0, NVMe® 2.0 specification compliant • Open Compute Project Datacenter NVMe™ SSD specification V2.0 support (not all requirements) • Error Vector Self-Test (EVSF) 3.6 error threshold • Proprietary ECC/BA architecture controller, firmware and BIOS FLASH™ generation 5 TLC flash • 100% drive-to-drive replication • Consistent performance and reliability for demanding 544K environments • 100% data integrity • Power loss protection (PLP) and end-to-end data correction • 100% 100% 100% 	<ul style="list-style-type: none"> • Hyperscale • IoT and big data analytics • Critical transaction processing (OLTP) • Operational and relational databases • Distributed architectures • Streaming media and content delivery • Cloud storage

Specifications

Basic Specifications	

Form Factor	2.5-inch, 15mm thickness
Interface	PCIe® 5.0 M.2™ 2280

Interface	PCIe 5.0, NVMe 2.0
Maximum Interface Speed	128 GT/s (PCIe® Gen5 x4)

Děkuji za pozornost

